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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,460	11/03/2003	Naoki Makita	70404.10	3457

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EXAMINER	
ANYA, IGWE U	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 05/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/699,460	MAKITA ET AL.	
	Examiner	Art Unit	
	Igwe U. Anya	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-68* is/are pending in the application.

4a) Of the above claim(s) *1-32 and 61-68* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *33-35 and 40-60* is/are rejected.

7)☒ Claim(s) *36-39,44 and 51* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/3/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 33 - 60 in the reply filed on March 4, 2005 is acknowledged.

Claim Objections

2. In claim 44 lines 4 – 5, "the second heat treatment", and in claim 51 lines 2 – 3, "one of the impurity element and the at least one of the rare gas element" are objected for lack of antecedent basis. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 33 – 35, 40, 41, 43 – 47, 51 – 53, and 56 – 60 are rejected under 35 U.S.C. 102(b) as being anticipated by Gotoh et al. (USPAB 2002/0149017).

5. Gotoh et al. teach a method for manufacturing a semiconductor film, comprising the steps of:

(a) forming an amorphous semiconductor layer (12) on an insulating surface (11);

(b) adding a catalyst element capable of promoting crystallization to the amorphous semiconductor layer and then performing a first heat treatment so as to crystallize the amorphous semiconductor layer, thereby obtaining a crystalline semiconductor layer (paragraph 95);

(c) performing a first gettering process to remove the catalyst element from the semiconductor layer (paragraph 99);

(d) performing a second gettering process that is different from the first gettering process to remove the catalyst element from the semiconductor layer (paragraph 101).

wherein the step (c) includes removing at least large masses of a semiconductor compound of the catalyst element present in the crystalline semiconductor layer (paragraph 101);

wherein the step (d) includes moving at least a part of the catalyst element remaining in the crystalline semiconductor layer so as to form a low-catalyst concentration region in the crystalline semiconductor layer, the low-catalyst-concentration region having a lower catalyst element concentration than in other regions (paragraph 101);

wherein the step (d) includes a step of moving the catalyst element present in a form of solid solution in the crystalline semiconductor layer (paragraphs 95 – 103);

wherein the step (c) includes a step of selectively etching away a semiconductor compound of the catalyst element (paragraphs 101 – 103);

wherein the step (d) includes a step of dissolving, in the crystalline semiconductor film, the catalyst element forming a semiconductor compound of the catalyst element remaining in the crystalline semiconductor film (paragraphs 95);

wherein the step (d) includes a step of forming a gettering region or a gettering layer capable of attracting the catalyst element, and a step of performing the second

heat treatment so that the catalyst element remaining in the crystalline semiconductor film is moved into the gettering region or the gettering layer (paragraph 101);

wherein the gettering region or the gettering layer has a larger amorphous component content than in other regions of the crystalline semiconductor film (paragraph 95);

wherein the gettering region or the gettering layer includes a group VB impurity element giving n-type conductivity selected from the group consisting of P, As and Sb (paragraph 99);

wherein at least one of the impurity element and the at least one rare gas element included in the gettering region or the gettering layer are introduced by an ion implantation method (paragraph 99);

further comprising a step of removing the gettering region or the gettering layer after the step (d) (paragraphs 101 – 103);

wherein the step (b) includes a step of selectively adding the catalyst element to a region of the amorphous semiconductor film-and then performing the first heat treatment so that a crystal growth process proceeds laterally from the region to which the catalyst element has been selectively added (paragraph 95);

wherein the step (b) includes a step of forming an insulating film on the crystalline semiconductor film after the first heat treatment step, the step (c) includes a step of selectively etching away a semiconductor compound of the catalyst element, and the etching step is performed after the first heat treatment step and before the

insulating film formation step in the step (b), and serves also as a surface cleaning step (paragraphs 97 – 101).

wherein the catalyst element is at least one metal element selected from the group consisting of Ni, Co, Sn, Pb, Pd, Fe and Cu (paragraph 95);

producing a thin film transistor including the semiconductor film in the active region thereof (paragraphs 103 – 109);

the active region includes a channel region, a source region and a drain region, and the step of producing the thin film transistor includes a step of forming at least the channel region in the low-catalyst-concentration region (paragraphs 103 – 109); and

wherein the step of producing the thin film transistor includes a step of forming the channel region, the source region and the drain region in the low-catalyst concentration region (paragraphs 103 – 109).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 48 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gotoh et al. (USPAB 2002/0149017).

9. Gotoh et al. teach the features previously outlined, but lack the steps wherein the gettering region or the gettering layer includes a group IIIB impurity element giving P-type conductivity, and wherein the impurity element includes at least one of B and Al.

10. However, Gotoh et al. teach an NMOS, and inferred a PMOS transistor can be manufactured by same process (paragraph 91).

11. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the steps wherein the gettering region or the gettering layer is a group IIIB impurity element giving P-type conductivity, and wherein the impurity element includes at least one of B and Al to form a PMOS.

12. Claims 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gotoh et al. (USPAB 2002/0149017) in view of Yamazaki et al. (US Patent 5608232).

13. Gotoh et al. teach the features previously outlined, but lack etching with hydrogen fluoride.

14. However, Yamazaki et al. teach etching with hydrogen fluoride for selectivity (col. 14 lines 52 – 59).

15. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Yamazaki et al. '232 into the Gotoh et al. reference for etch selectivity.

16. Claims 50, 54 and 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gotoh et al (USPAB 2002/0149017) in view of Yamazaki et al. (USPAB 2002/0197785).

17. Gotoh et al. teach the features previously outlined, but lack the steps wherein:

the gettering region or the gettering layer includes at least one rare gas element selected from the group consisting of Ar, Kr and Xe;

wherein at least one of the impurity element and the at least one rare gas element included in the gettering region or the gettering layer are introduced by an ion implantation method (paragraph 99);

step (b) includes a step of irradiating the crystalline semiconductor film with laser light after the first heat treatment; and

step (c) includes a step of selectively etching away a semiconductor compound of the catalyst element, and the etching step is performed after the first heat treatment step and before the laser light irradiation step in the step (b), and serves also as a surface cleaning step.

18. However, Yamazaki et al. teach the steps wherein:

the gettering region or the gettering layer includes at least one rare gas element selected from the group consisting of Ar, Kr and Xe (paragraph 117) to increase the etching ratio of the amorphous film to the crystalline film (paragraph 113);

at least one of the impurity element and the at least one rare gas element included in the gettering region or the gettering layer are introduced by an ion implantation method (paragraphs 111, 113);

step (b) includes a step of irradiating the crystalline semiconductor film with laser light after the first heat treatment (figs. 2A – 2D) to increase the crystallinity of the crystalline film (paragraph 107); and

step (c) includes a step of selectively etching away a semiconductor compound of the catalyst element, and the etching step is performed after the first heat treatment step and before the laser light irradiation step in the step (b), and serves also as a surface cleaning step (figs. 2A – 2D).

19. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Yamazaki et al. '785 into the Gotoh et al. reference for optimization.

20. Claims 36 – 39 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Igwe U. Anya whose telephone number is (571) 272-1887. The examiner can normally be reached on M - F 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William B. Baumeister can be reached on (571) 272-1722. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Igwe U. Anya
Examiner
Art Unit 2891

IA

April 26, 2005